Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.022”**

**SOURCE**

**GATE**

**.018”**

**Top Material: Al**

**Backside Material: Au**

**S = .006” X .007”**

**G = .004” X .004”**

**Backside Potential: DRAIN**

**APPROVED BY: DK DIE SIZE .018” X .022” DATE: 9/23/21**

**MFG: SILICON SUPPLIES THICKNESS .008” P/N: BS170**

**DG 10.1.2**

#### Rev B, 7/19/02